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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,983	08/29/2001	Hiroaki Fujii	NIT-2952	5977

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EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,983	FUJII ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/29/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the communication filed on 8/29//2001.

Claims 1-13 are pending in the application.

Information Disclosure Statement

2. Some contents of information disclosure statement filed on 8/29/01, which are not marked with initials, fail to comply with the requirements under 37 CFR 1.98(a)(5): Each publication listed in an information disclosure statement must be identified by publisher, author (if any), title, relevant pages of the publication, date, and place of publication.

It has been placed in the application file, but the contents referred to therein have not been considered. See MPEP 609.

Specification

3. The abstract of the disclosure is objected to because content of the abstract exceeds more than 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-7, 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per Claim 1:

The claimed limitation "*a processing flow for translating respective of the instructions into an instruction binary code understandable by itself when necessary,*" is indefinite because the functionality of the claim is unclear. What is "itself"? What kind of code is it *understandable by itself*?

Examiner interprets that native code that is understandable by its own processor.

As per Claims 2-7: Claims 2-7 are dependent on the indefinite Claim 1. Therefore, the claims are indefinite because of dependency.

As per Claim 13:

The claimed preamble "*A binary translation program for making a computer perform in parallel:*" is indefinite because the meaning is unclear. What does it mean, "*making a computer perform in parallel*? Since the phrase *for making a computer perform in parallel* is unclear, Examiner interprets that the preamble is intended to a program per se.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. The claim 13 is rejected under 35 U.S.C 101 because the claimed invention is directed to non-statutory subject matter.

As per claim 13: Claim 13 is claiming a binary translation program and fails to cause the claim to be tangibly embodied. The words "for performing", "for translating" and "for executing" followed after the limitations 'a step's are rather the labels of the ' a step's that are interpreted as modules in the program,

than hardware tangibility. Claim 13's steps could be identified as programming modules implemented in a paper. Such claim fails to be in the technological or useful arts and thus fails to recite patent eligible subject matters.

According to the analysis above, claim 13 is claiming software modules that are not tangible in computer hardware for causing the computer to execute in a practical manner. Claim 13 thus is programming per se and held nonstatutory.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. 101 (nonstatutory) above is further rejected as set forth below in anticipation of application amending this claim to place it within the four statutory categories of invention.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 1-4, 6-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Zheng et al, "PA-RISC to IA-64: Transparent Execution, no Recompilation", IEEE 3-2000 (hearafter Zheng).

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per claim 1: Zheng discloses

A processor system that includes a dynamic translation facility and that runs a binary-coded program oriented to an incompatible platform while dynamically translating instructions, which constitute the program, into instruction binary codes understandable by itself, comprising:

a processing flow for fetching the instructions, which constitute the binary-coded program oriented to an incompatible platform, one by one, and interpreting the instructions one by one using software (See page 49, Figure 2, "Start", *fetching the instructions*; See page 48, Figure 1, "HP-UX on IA-64", *binary-coded program oriented to an incompatible platform*; "Fast interpreter" and "Aries runtime module", *interpreting the instructions one by one using software*); *and*

a processing flow for translating respective of the instructions into an instruction binary code understandable by itself when necessary, storing the instruction binary code, and optimizing the instruction binary code being stored when necessary (See page 49, Figure 2, "start",..., "translated code cache", *translating respective of the instructions into an instruction binary code understandable by itself when necessary, storing the instruction binary code*; see page 50, left column, section "Optimizer and Schedule", *optimizing*),

wherein: the processing flow for interpreting the instructions and the processing flow for translating are independent and processed in parallel with each other (See Figure 1, "Fast interpreter" and "Dynamic translator" *processed in parallel with each other*).

As per claim 2: Zheng discloses, "*A processor system according to claim 1, wherein: during optimization of respective instruction binary code, new instruction binary codes are arranged to produce a plurality of processing flows so that iteration or procedure call can be executed in parallel with each other*" (See page 50, section "Optimizer and Schedule", *during optimization*; and see details of Figure 2 (beneath Figure 2. referring to "run-time module switch control".

As per Claim 3: Zheng discloses, "*A processor system according to claim 1, wherein: a processing flow for prefetching the binary-coded program oriented to the incompatible platform into a cache memory is defined separately from the processing flow for interpreting and the processing flow for translating and optimizing; and the processing flow for prefetching is processed in parallel with the processing flow for interpreting and the processing flow for translating and optimizing*" (See page 49, Figure 2 and Figure 2's details, "Translated code cache" and "...and address map table to determine whether or not Aries has translated the target block into dyncode (translated code containing native IA-64 instructions", *a*

processing flow for prefetching; See "translation exist?" and "interpret until branch", *interpreting and the processing*).

As per Claim 4: Zheng discloses "*A processor system according to claim 1, wherein: every time translation and optimization of an instruction binary code of a predetermined unit is completed within the processing flow for translating and optimizing, the optimized and translated instruction binary code is exchanged for an instruction code that is processed within the processing flow for interpreting at the time of completion of optimization; and when the instructions constituting the binary-coded program oriented to the incompatible platform are being interpreted one by one within the processing flow for interpreting, in case that an optimized translated instruction binary code corresponding to one instruction is present, the optimized translated instruction binary code is executed*" (See the whole process (beneath Figure 2) explained for Figure 2).

As per Claim 6: Zheng discloses "*A processor system according to claim 1, wherein one instruction execution control unit processes a plurality of processing flows concurrently, and the plurality of processing flows are processed in parallel with one another*" (See Figure 1).

As per Claim 7: Zheng discloses, *A processor system according to claim 1, wherein when a translated instruction being processed within the processing flow for interpreting is exchanged for a new translated instruction produced by optimizing the translated instruction within the processing flow for translating and optimizing, an exclusive control is performed* (See Figure 2, "runtime module switches control"; and see page 50, left column, section "Optimizer and Schedule", *optimizing*).

As per Claim 8: Zheng discloses:

A processor system including a dynamic translation facility and including at least one processing flow, wherein: the at least one processing flow includes a first processing flow for sequentially prefetching a plurality of instructions, which constitute a binary-coded program to be run in incompatible hardware, and storing the instructions in a common memory (See page 49, Figure 2 and Figure 2's details, "Translated code cache" *prefetching*), *a second processing flow for concurrently interpreting the plurality of instructions stored in the common memory in parallel with one another* (See page 49, Figure 2 and Figure 2's details, "interpret until branch" *second processing flow*), *and a third processing flow for*

translating the plurality of interpreted instructions (See page 49, Figure 2 and Figure 2's details, "Translation exists?", *third processing flow*).

As per Claim 9: Zheng discloses, *A processor system according to claim 8, wherein the second processing flow executes the translated code when the instruction of the plurality of instructions have already been translated and interprets the instruction when it has not been translated* (See Figure 2 details (beneath Figure 2)).

As per Claim 10: Zheng discloses, "*A processor system according to claim 8, wherein within the third processing flow, among the plurality of instructions, instructions that have not been translated are translated, and the translated instructions are re-sorted or the number of translated instructions is decreased*" (See Figure 2 details (beneath Figure 2)).

As per Claim 11: Regarding claimed limitation: *A processor system according to claim 8, wherein the first processing flow, the second processing flow, and the third processing flow are processed independently in parallel with one another* (See Figure 1 and Figure 2).

As per Claim 12: Regarding claimed limitation, *A semiconductor device having at least one microprocessor, a bus, and a common memory, including: the at least one microprocessor composed of processing at least one processing flow; the at least one processing flow including: a first processing flow for sequentially prefetching a plurality of instructions that constitute a binary-coded program to be run in incompatible hardware, and storing the instructions in the common memory, a second processing flow for concurrently interpreting the plurality of instructions stored in the common memory in parallel with one another, and a third processing flow for translating the plurality of interpreted instructions, wherein: the at least one microprocessor is composed of implementing the plurality of instructions in parallel with one another*: (See rationale in Claim 8 above).

As Per Claim 13: Zheng discloses:

A binary translation program for making a computer perform in parallel: a step for performing fetching of a plurality of instructions into the computer; a step for translating instructions, which have not been translated, among the plurality of instructions; and a step for executing the instructions through the step for translating (see Figure 2).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zheng et al, "PA-RISC to IA-64: Transparent Execution, no Recompilation", IEEE 3-2000, in view of Hammond et al., "Data Speculation Support for a Chip Multiprocessor", ACM 1998 (hearafter: Hammond).

As per Claim 5: Regarding limitation: "*A processor system according to claim 1, wherein the processor system is implemented in a chip multiprocessor that has a plurality of microprocessors mounted on one LSI chip, and the different microprocessors process the plurality of processing flows in parallel with one another*"

Zheng does not explicitly address *has a plurality of microprocessors mounted on one LSI chip,*

Hammond discloses processors that are implemented in a chip and *process the plurality of processing flows in parallel with one another* (See Hammond, Abstract, "Chip Multiprocessor" and "parallelism").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to extend the PA-RICS and IA-64 architecture of Zheng to architecture Chip Multiprocessor of Hammond. Doing so would be beneficial to microprocessor performances.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Uhlig et al., "Instruction Fetching: Coping With Code Bloat", ACM 1995, discloses an improvement of instruction fetch performance.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be reached on Monday-Friday from 8:00 AM to 5:30 PM ET. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam, can be reached on (703) 305-4552.

The fax phone numbers:

(703) 872-9306 (for formal communication intended for entry);

(703) 746-5429 (for informal or draft communication, please label "PROPOSED" or "DRAFT").

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TED T. VO
Patent Examiner
Art Unit: 2122
June 10, 2004